

Robust Design Verification

Capturing noise with the P-diagram, verifying it with a design matrix, and closing the loop with robust parameter design

Khalid Mekki, PhD — Master Black Belt, Design for Six Sigma & Lean Six Sigma
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Executive summary

Most verification plans confirm that a design works at nominal. That is the least useful thing to know. This paper walks through the discipline that closes the gap between "passes at nominal" and "survives in the field": building a P-diagram to make noise a first-class design input, using a design verification (DV) matrix to trace every noise factor into an actual test result, and running a robust parameter design experiment to fix what verification flags as marginal — rather than simply re-testing it and hoping. A worked example, an enclosure door latch assembly, illustrates each step with real numbers.

1. The P-diagram: noise as a first-class design input

A P-diagram (Parameter Diagram) is not a documentation exercise — it is a noise-hunting discipline. Its structure is simple: a signal enters a system and produces a response, shaped by control factors the design team can set and noise factors it cannot. The value is not the box diagram itself. The value is that it forces an explicit answer to the question every DFMEA and verification plan quietly assumes has already been answered — what is actually going to act on this design once it leaves the CAD model.

Why it belongs in verification

The P-diagram's real payoff shows up downstream, in two places. First, it feeds the DFMEA: every noise factor is a candidate cause for a failure mode, and a DFMEA built without a preceding P-diagram tends to capture only the causes the team already knows about. Second, it shapes the design verification plan: each noise factor, or a deliberately harsh combination of several, should become a stress condition in the test matrix. If a noise factor is on the P-diagram but has no corresponding line in the verification plan, that is not a documentation gap — it is an unverified failure mode wearing a disguise.

The noise buckets

- **Piece-to-piece variation** — tolerances, material batch variation, supplier drift.
- **Changes over time** — wear, fatigue, creep, corrosion, seal relaxation.
- **Customer usage** — actual duty cycle, overload, off-label use, edge-case operators.
- **External environment** — temperature, humidity, vibration, EMI, altitude, contamination.

- **System interaction** — noise injected by adjacent subsystems: shared power rails, thermal coupling, mechanical loading.

Teams reliably fill in piece-to-piece and environment, because both are familiar and testable in a lab. Usage and system interaction get thin, because they require talking to field service, warranty, and other subsystem owners instead of running a chamber test — and those two buckets are disproportionately where real-world failures come from.

Practical rules

- Build the P-diagram before the DFMEA, not after, so causes are drawn from a disciplined noise inventory rather than generic engineering guesses.
- Involve manufacturing, field service, and owners of interfacing systems — design engineering alone will not surface usage or interaction noise.
- For every noise factor, ask how it would be replicated in a test. An unanswerable question is a verification gap, not a finished row.
- Compound noises deliberately — test the worst reasonable combination together, not each noise independently at nominal-plus-margin.
- Aim for desensitization, not elimination — tune control factors so the response stays on target despite the noise, rather than trying to design the noise away.
- Treat it as a living document — every test failure or field return that traces to a cause not on the list is a signal to update it, and to check whether the DFMEA and verification plan inherited the gap.

A P-diagram that isn't traceable into the DFMEA's causes and the verification plan's test conditions is a poster, not a robustness tool.

2. Worked example: enclosure door latch, Rev C

The matrix below is an illustrative example, not field data. It shows how four critical-to-quality responses trace through their control-factor settings, their sensitivity to each noise category, and the test result that actually matters — the worst-case compound condition, not the nominal one.

#	CTQ characteristic / target	Control factors	Noise sensitivity (P2P · time · use · env · interact.)	Test method / n	Nominal	Worst-case compound	Cpk	Status
1	Latch engagement force 25–45 N	Arm 1.8 mm · preload 12 N · cam 32° · pin ø4.0 mm	H · M · H · M · L	Force-gauge pull, n=30	34 N	26 N	1.42	Pass
2	Seal compression retention ≥ 0.80 mm deflection	Arm 1.8 mm · cam 32° · seal durometer 60A	M · H · M · H · M	IEC 60529 ingress, n=15	1.10 mm	0.72 mm	0.91	Watch
3	Hinge cycle life ≥ 50,000 cycles	Pin ø4.0 mm · preload 12 N · bushing POM	L · H · H · M · L	Cyclic life rig, n=8	82,000	51,200	1.05	Pass
4	Closure flush gap 0.5 mm ± 0.3	Arm 1.8 mm · cam 32° · pin ø4.0 mm · durometer 60A	H · M · L · M · H	Optical gap scan, n=25	0.48 mm	0.71 mm	0.88	Watch

H / M / L = high / medium / low sensitivity to that noise category. Pass = meets target under worst-case compound noise. Watch = marginal Cpk — a control-factor tuning candidate for the robust parameter design step in Section 3.

Noise factors — values applied in test

Noise category	Description and value applied in test
Piece-to-piece	Component tolerance and material-batch variation. Applied: ±3σ tolerance stack, per process capability data.
Time / wear	Spring fatigue, seal relaxation, bushing wear. Applied: accelerated cycling to 5-year field-life equivalent.
Customer use	Operating force, frequency, slam-close misuse. Applied: 10th–90th percentile field data plus a slam-close outlier.
Environment	Temperature, humidity, vibration, ingress. Applied: −30°C to 85°C · 95% RH · IEC 60529 spray.
System interaction	Load coupled in from adjacent panel and frame. Applied: +15°C conducted rise · ±0.2 mm frame deflection.

Rows 2 and 4 share cam angle and seal/arm dimensions as their most sensitive control factors — that overlap is the priority signal for the robustness experiment in Section 3, not a coincidence to note and move past.

3. From verification to robust design: closing the loop with DOE

The P-diagram shows where the noise is. The DV matrix shows which characteristics are sensitive to it. Neither one fixes anything. A "Watch" status — rows 2 and 4 above — is a diagnosis, not a resolution. The next step is a robust parameter design experiment, and it is the step most often skipped because it looks like extra work once the schedule already says "we tested it."

A normal experiment asks which control factors move the response, and by how much. A robust parameter design experiment asks a sharper question: which control-factor setting makes the response stop caring about the noise? That means varying noise factors deliberately inside the same experiment — control factors in an inner array, noise factors in an outer array — and looking for the setting where the response stays flat across noise levels, not just the setting that hits target at nominal.

This distinction matters because two control-factor settings can both hit the target mean and still be different designs. One reaches 0.50 mm nominal but swings 0.30–0.75 mm across the noise array; another reaches 0.52 mm nominal but only swings 0.44–0.58 mm across the same array. A verification plan that only checks nominal calls both of these a pass. Variance across noise, not distance from target, is what turns into field failures.

Running the experiment

- Put only the sensitive control factors in the inner array — the DV matrix already identified them. For the latch example, that is cam angle and seal durometer.
- Use the same noise levels already defined in the P-diagram and verification plan — inventing new ones here throws away the traceability already built.
- Look for a control factor that reduces variance without moving the mean, and a separate factor that adjusts the mean without adding sensitivity — that pairing is the core trick of robust parameter design.
- Confirm the recommended setting with a run at the exact worst-case compound condition that produced the original "Watch," not just the experiment's own design points.
- Feed the result back into the DFMEA and verification plan, not only the drawing — the reduced sensitivity is new evidence for the occurrence rating.

Verification tells you a design is sensitive to noise. Robust parameter design is the step that makes it stop being sensitive — chasing the mean without measuring variance across noise just produces a design that passes today's test and fails next year's field conditions.

Key takeaways

- The P-diagram makes noise a design input, not a field discovery.
- The DV matrix is only meaningful if it traces to a worst-case compound test result, not a nominal one.

- A "Watch" status is an instruction to run a robust parameter design experiment, not to retest and hope.

About the author

Khalid Mekki, PhD is the founder of Design for Lean and one of a small number of consultants worldwide holding Master Black Belt certification in both Design for Six Sigma and Lean Six Sigma. He brings more than 30 years of operational excellence experience across Baxter Healthcare, AstraZeneca—Medimmune Biologics, and Ford Motor Company, and co-authored the first published book on Design for Six Sigma for the medical device industry (2008). He holds a PhD in Industrial Engineering and Operations Research from the University of Illinois at Chicago, an MSc in Manufacturing from the University of Detroit Mercy, and a BSc in Mechanical Engineering from Palestine Polytechnic University.

designforlean.com · kmekki@gmail.com